



PATENT  
Attorney Docket No. ASC-061

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S): Lochtefeld et al.

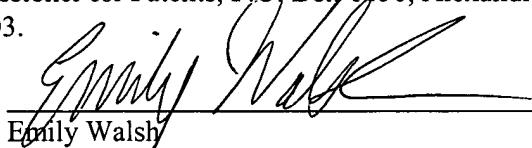
SERIAL NO.: 10/629,498 GROUP NO.: Not Yet Assigned

FILING DATE: July 29, 2003 EXAMINER: Not Yet Assigned

TITLE: SELECTIVE PLACEMENT OF DISLOCATION ARRAYS

**CERTIFICATE OF FIRST CLASS MAILING UNDER 37 C.F.R. 1.8**

I hereby certify that this correspondence, and any document(s) referred to as enclosed herein, is/are being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 31<sup>st</sup> day of October, 2003.



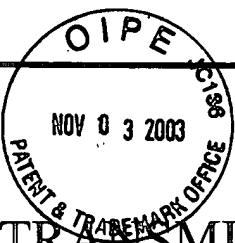
Emily Walsh

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Submitted herewith are:

1. Transmittal Form (1 pg.);
2. Supplemental Information Disclosure Statement (2 pgs.);
3. Supplemental Form PTO-1449 (7 pgs.);
4. Copies of Cited References (C4-C37);
5. Return Receipt Postcard; and this
6. Certificate of First Class Mailing (1 pg.).



**TRANSMITTAL  
FORM**

Application Serial Number	10/629,498
Filing Date	July 29, 2003
First Named Inventor	Lochtefeld
Group Art Unit	Not Yet Assigned
Examiner Name	Not Yet Assigned
Attorney Docket No.	ASC-061
Patent No.	Not Applicable
Issue Date	Not Applicable

**ENCLOSURES (check all that apply)**

<input type="checkbox"/> Fee Transmittal Form <ul style="list-style-type: none"> <li><input type="checkbox"/> Check Attached</li> <li><input type="checkbox"/> Copy of Fee Transmittal Form</li> </ul>	<input type="checkbox"/> Copy of Notice to File Missing Parts of Application	<input type="checkbox"/> Notice of Appeal to Board of Patent Appeals and Interferences
<input type="checkbox"/> Amendment/Response <ul style="list-style-type: none"> <li><input type="checkbox"/> Preliminary</li> <li><input type="checkbox"/> After Final</li> <li><input type="checkbox"/> Affidavits/declaration(s)</li> <li><input type="checkbox"/> Letter to Official Draftsperson including Drawings</li> <li>[Total Sheets _____]</li> </ul>	<input type="checkbox"/> Formal Drawings	<input type="checkbox"/> Appeal Brief (in triplicate)
	<input type="checkbox"/> Request For Continued Examination (RCE) Transmittal	<input type="checkbox"/> Status Inquiry
	<input type="checkbox"/> Power of Attorney (Revocation of Prior Powers)	<input checked="" type="checkbox"/> Return Receipt Postcard
	<input type="checkbox"/> Terminal Disclaimer	<input checked="" type="checkbox"/> Certificate of First Class Mailing under 37 C.F.R. 1.8
<input type="checkbox"/> Petition for Extension of Time	<input type="checkbox"/> Executed Declaration and Power of Attorney for Utility or Design Patent Application	<input type="checkbox"/> Certificate of Facsimile Transmission under 37 C.F.R. 1.8
<input checked="" type="checkbox"/> Supplemental Information Disclosure Statement <ul style="list-style-type: none"> <li><input checked="" type="checkbox"/> Supplemental Form PTO-1449</li> <li><input checked="" type="checkbox"/> Copies of IDS Citations (C4-C37)</li> </ul>	<input type="checkbox"/> Small Entity Statement	<input type="checkbox"/> Additional Enclosure(s) (please identify below)
<input type="checkbox"/> Certified Copy of Priority Document(s)	<input type="checkbox"/> CD(s) for large table or computer program	
<input type="checkbox"/> Sequence Listing submission <ul style="list-style-type: none"> <li><input type="checkbox"/> Paper Copy/CD</li> <li><input type="checkbox"/> Computer Readable Copy</li> <li><input type="checkbox"/> Statement verifying identity of above</li> </ul>	<input type="checkbox"/> Amendment After Allowance	
	<input type="checkbox"/> Request for Certificate of Correction <ul style="list-style-type: none"> <li><input type="checkbox"/> Certificate of Correction (in duplicate)</li> </ul>	

**CORRESPONDENCE ADDRESS**

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 Testa, Hurwitz & Thibeault, LLP  
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 125 High Street  
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**SIGNATURE BLOCK**

Respectfully submitted,

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PATENT  
Attorney Docket No. ASC-061

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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FILING DATE: July 29, 2003 EXAMINER: Not Yet Assigned

TITLE: SELECTIVE PLACEMENT OF DISLOCATION ARRAYS

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

Sir:

In accordance with the provisions of 37 C.F.R. 1.97 and 1.98, Applicants hereby make of record the patents and publications listed on the accompanying Form PTO-1449, and other information contained herein, for consideration by the Examiner in connection with the examination of the above-identified patent application. Copies of the publications are enclosed.

**REMARKS**

In accordance with the provisions of 37 C.F.R. 1.97, this statement is being filed (CHECK ONE):

- (1) within three (3) months of the **filings date** of a national application other than a continued prosecution application under 37 C.F.R. 1.53(d), or within three (3) months of the **date of entry of the national stage** as set forth in 37 C.F.R. 1.491 in an international application, or before the mailing of the **first Office action** on the merits, or before the mailing of a **first Office action** after the filing of a request for continued examination under 37 C.F.R. 1.114; or
- (2) after the period defined in (1) but before the mailing date of a **final action** or a **notice of allowance** under 37 C.F.R. 1.311, and
- the requisite Statement is below, **OR**

- the requisite fee under 37 C.F.R. 1.17(p), namely **\$180.00**, is included herein, or
- (3) after the mailing date of a **final action or notice of allowance** but before the payment of the **issue fee**, **AND**
  - the requisite Statement is below, **AND**
  - the requisite petition fee under 37 C.F.R. 1.17(p), namely **\$180.00** is included herein.

It is respectfully requested that each of the patents and publications listed on the attached Form PTO-1449, and other information contained herein, be made of record in this application.

In addition, Applicants wish to inform the Examiner about the following co-pending patent applications, including all Office actions issued therein:

U.S. Serial No. 10/264,935, filed on October 4, 2002, by Lochtefeld et al.

U.S. Serial No. 10/456,708, filed on June 6, 2003, by Lochtefeld et al.

U.S. Serial No. 10/456,103, filed on June 6, 2003, by Lochtefeld et al.

Respectfully submitted,

Date: October 31, 2003  
Reg. No. 44,381

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<b>FORM PTO - 1449</b>		ATTY DOCKET NO.	ASC-061
<b>SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT</b>		APPLICANTS:	Lochtefeld et al.
		SERIAL NO.:	10/629,498
		FILING DATE:	July 29, 2003
		GROUP:	Not yet assigned

#### U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A2	4,885,614	12/5/1989	Furukawa et al.			
	A3	5,032,893	7/16/1991	Fitzgerald et al.			
	A4	5,084,411	1/28/1992	Laderman et al.			
	A5	5,091,767	2/25/1992	Bean et al.			
	A6	5,156,995	10/20/1992	Fitzgerald et al.			
	A7	5,256,550	10/26/1993	Laderman et al.			

#### FOREIGN PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)

#### OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
	C4	Akatsu et al., "Wafer bonding of different III-V compound semiconductors by atomic hydrogen surface cleaning," <u>Journal of Applied Physics</u> , Vol. 90, No. 8 (October 15, 2001), pp. 3856-3862.
	C5	Belgal et al., "A New Mechanism of Pipeline Defect Formation in CMOS Devices," <u>International Reliability Physics Symposium</u> , (1994), pp. 399-404.
	C6	Bulsara et al., "Relaxed In <sub>x</sub> Ga <sub>1-x</sub> As graded buffers grown with organometallic vapor phase epitaxy on GaAs," <u>Applied Physics Letters</u> , Vol. 72, No. 13 (March 30, 1998), pp. 1608-1610.
	C7	Cullis et al., "Growth ripples upon strained SiGe epitaxial layers on Si and misfit dislocation interactions," <u>Journal of Vacuum Science and Technology</u> , A 12(4) (July/August 1994), pp. 1924-1931.
	C8	Currie et al., "Carrier mobilities and process stability of strained Si n- and p-MOSFETs on SiGe virtual substrates," <u>Journal of Vacuum Science and Technology</u> , B 19(6) (November/December 2001), pp. 2268-2279.

<b>EXAMINER</b>	<b>DATE CONSIDERED</b>
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EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A8	5,323,031	6/21/1994	Shoji et al.			
	A9	5,659,187	8/19/1997	Legoues et al.			
	A10	5,801,085	9/1/1998	Kim et al.			
	A11	5,810,924	9/22/1998	Legoues et al.			
	A12	5,828,114	10/27/1998	Kim et al.			
	A13	5,937,274	8/10/1999	Kondow et al.			

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#### OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
	C9	De Boeck et al., "Growth and structural characterization of embedded InAsSb on GaAs-coated patterned silicon by molecular beam epitaxy," <u>Applied Physics Letters</u> , 58 (9) (March 4, 1991), pp. 928-930.
	C10	Feenstra et al., "Scattering from strain variations in high-mobility Si/SiGe heterostructures," <u>Journal of Applied Physics</u> , 78 (10) (November 15, 1995), pp. 6091-6097.
	C11	Fitzgerald et al., "Dislocation dynamics in relaxed graded composition semiconductors," <u>Materials Science and Engineering</u> , B67 (1999), pp. 53-61.
	C12	Godbey et al., "A Si0.7Ge0.3 strained-layer etch stop for the generation of thin layer undoped silicon," <u>Applied Physics Letters</u> , 56 (4) (January 22, 1990), pp. 373-375.
	C13	Gonzales et al., "Advantages of thin interfaces in step-graded buffer structures," <u>Materials Science and Engineering</u> , B44 (1997), pp. 41-45.

EXAMINER	DATE CONSIDERED



<b>FORM PTO - 1449</b> <b>SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT</b>					ATTY DOCKET NO. ASC-061 APPLICANTS: Lochtefeld et al. SERIAL NO.: 10/629,498 FILING DATE: July 29, 2003 GROUP: Not yet assigned				
<b>U.S. PATENT DOCUMENTS</b>									
EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME		CLASS	SUB CLASS	FILING DATE IF APPROPRIATE	
	A14	6,576,532	6/10/2003	Jones et al.					
	A15	US 20020185686A	12/12/2002	Christiansen et al.					
<b>FOREIGN PATENT DOCUMENTS</b>									
EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
<b>OTHER ART, JOURNAL ARTICLES, ETC.</b>									
EXAM. INIT.	<b>OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)</b>								
	C14	Gray et al., "Effect of Anisotropic Strain on the Crosshatch Electrical Activity in Relaxed GeSi Films," <u>Physical Review Letters</u> , Vol. 86, No. 16 (April 16, 2001), pp. 3598-3601.							
	C15	Ha et al., "Anomalous Junction Leakage Current Induced by STI Dislocations and Its Impact on Dynamic Random Access Memory Devices," <u>IEEE Transactions on Electron Devices</u> , Vol. 46, No. 5 (May 1999), pp. 940-946.							
	C16	Knall et al., "The use of graded InGaAs layers and patterned substrates to remove threading dislocations from GaAs on Si," <u>Journal of Applied Physics</u> , 76 (5) (September 1, 1994), pp. 2697-2702.							
	C17	MacElwee et al., "High-Performance Fully Depleted Silicon-on-Insulator Transistors," <u>IEEE Transactions on Electron Devices</u> , Vol. 37, No. 6 (June 1990), pp. 1444-1451.							
<b>EXAMINER</b>					<b>DATE CONSIDERED</b>				



<b>FORM PTO - 1449</b>  <b>SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT</b>					<b>ATTY DOCKET NO.</b> ASC-061  <b>APPLICANTS:</b> Lochtefeld et al. <b>SERIAL NO.:</b> 10/629,498 <b>FILING DATE:</b> July 29, 2003 <b>GROUP:</b> Not yet assigned				
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EXAM. INIT.	<b>OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)</b>								
	C18	McCarthy et al., "Effect of threading dislocations on AlGaN/GaN heterojunction bipolar transistors," <u>Applied Physics Letters</u> , Vol. 78, No. 15 (April 9, 2001), pp. 2235-2237.							
	C19	Meshkinpour et al., "Role of misfit dislocations on pseudomorphic high electron mobility transistor," <u>Applied Physics Letters</u> , 66 (6) (February 6, 1995), pp. 748-750.							
	C20	Mica et al., "Crystal defects and junction properties in the evolution of device fabrication technology," <u>Journal of Physics: Condensed Matter</u> , 14 (2002), pp. 13403-13410.							
	C21	Momose et al., "Dislocation-free and lattice-matched Si/GaP <sub>1-x</sub> N <sub>x</sub> /Si structure for photo-electronic integrated systems," <u>Applied Physics Letters</u> , Vol. 79, No. 25 (December 17, 2001), pp. 4151-4153.							
	C22	Mooney et al., "Scanning x-ray microtopographs of misfit dislocations at SiGe/Si interfaces," <u>Applied Physics Letters</u> , Vol. 79, No. 15 (October 8, 2001), pp. 2363-2365.							
<b>EXAMINER</b>					<b>DATE CONSIDERED</b>				



## FORM PTO - 1449

SUPPLEMENTAL INFORMATION  
DISCLOSURE STATEMENT

ATTY DOCKET NO. ASC-061

APPLICANTS: Lochtefeld et al.

SERIAL NO.: 10/629,498

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## OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
	C23	Mooney et al., "SiGe TECHNOLOGY: Heteroepitaxy and High-Speed Microelectronics," <u>Annual Review of Materials Science</u> , 30 (2000), pp. 335-362.
	C24	Mooney et al., "Thermal Stability of Strained Si on Relaxed Si <sub>1-x</sub> Gex Buffer Layers," <u>Materials Research Society Symposium Proceedings</u> , Vol. 686 (2002), pp. A1.2.1-A1.2.6.
	C25	Morris et al., "Structure property anisotropy in lattice-mismatched single heterostructures," <u>Journal of Applied Physics</u> , 71 (5) (March 1, 1992), pp. 2321-2327.
	C26	Ohashi et al., "Simulation of dislocation accumulation in ULSI cells with STI structure," <u>Applied Surface Science</u> , (2003), pp. 1-7.
	C27	Rammohan et al., "Study of μm-scale spatial variations in strain of a compositionally step-graded In <sub>x</sub> Ga <sub>1-x</sub> /GaAs(001) heterostructure," <u>Applied Physics Letters</u> , 66 (7) (February 13, 1995), pp. 869-871.

EXAMINER

DATE CONSIDERED



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EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
	C28	Samavedam et al., "Novel dislocation structure and surface morphology effects in relaxed Ge/Si-Ge(graded)/Si structures," <u>Journal of Applied Physics</u> , 81 (7) (April 1, 1997), pp. 3108-3116.
	C29	Sleight et al., "Stress Induced Defects and Transistor Leakage for Shallow Trench Isolated SOI," <u>IEEE Electron Device Letters</u> , Vol. 20, No. 5 (May 1999), pp. 248-250.
	C30	Soh et al., "Relation Between Etch Pit Pairs And Pipeline Defects In CMOS Device," <u>International Reliability Physics Symposium</u> , pp. 244-248.
	C31	Su et al., "Effects of Dislocation and Bulk Micro Defects on Device Leakage," SEMICON Taiwan 2001, pp. 1-4.
	C32	Thompson et al., "NMOS Device Characteristics in Electron-Beam-Recrystallized SOI," <u>IEEE Transactions on Electron Devices</u> , Vol. 40, No. 7 (July 1993), pp. 1270-1276.

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<b>FORM PTO - 1449</b> <b>SUPPLEMENTAL INFORMATION</b> <b>DISCLOSURE STATEMENT</b>					ATTY DOCKET NO. ASC-061 APPLICANTS: Lochtefeld et al. SERIAL NO.: 10/629,498 FILING DATE: July 29, 2003 GROUP: Not yet assigned				
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	C33	Tromp et al., "ADVANCES IN SITU ULTRA-HIGH VACUUM ELECTRON MICROSCOPY: Growth of SiGe on Si," <u>Annual Review of Materials Science</u> , 30 (2000), pp. 431-449.							
	C34	Wang et al., "PIPELINE DEFECTS IN CMOS MOSFET DEVICES CAUSED BY SWAMI ISOLATION," <u>International Reliability Physics Symposium</u> , (1992), pp. 85-90.							
	C35	Williams et al., "Evaluation of the Yield Impact of Epitaxial Defects on Advanced Semiconductor Technologies, 2000 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp. 1-7.							
	C36	Wu, "Novel Etch-Stop Materials for Silicon Micromachining," Master of Science Thesis, Massachusetts Institute of Technology, 1997.							
	C37	Yamada et al., "Static analysis of off-axis crystal film growth onto a lattice-mismatched substrate," <u>Applied Physics Letters</u> , Vol. 79, No. 5 (July 30, 2001), pp. 608-610.							
<b>EXAMINER</b>					<b>DATE CONSIDERED</b>				